REMARKS

The present Amendment is being filed as a Submission pursuant to 37 C.F.R. §1.114. Acceptance of the same and withdrawal of the finality of the last Office Action in accordance with the U.S. PTO RCE procedure are respectfully requested. Reconsideration and withdrawal of the outstanding rejections is also requested.

Presently, each of the independent claims was amended to particularly define that in the erase operation the control module updates the designation of the nonvolatile semiconductor memory in the "table" after each occurrence of sending an erase command to a respective nonvolatile memory. Moreover, the independent claims further call for the control modules to execute status polling from the memory chip into which the erase command has been initially written as it relates to each of the successively sent first and second erase commands. Since both independent claims 1 and 16 now also call for the executing of status polling, although differently presented, claim 17 was accordingly cancelled but, however, without prejudice or disclaimer of the subject matter therein.

Several other revisions were implemented to the claims that are, generally, of an editorial formatting nature (see the first two 'wherein' clauses in claims 1 and 16). Also, in claim 1, line 3, thereof, the semicolon was replaced with a colon and in dependent claim 2, the expression "farther comprising" was corrected to the expression further comprising. In independent claim 16, further, "said each block...", in lines 4-5 thereof, was amended to the expression each block....

The present invention is a semiconductor storage apparatus which facilitates a highly efficient erasing of data operation of a plurality of nonvolatile semiconductor memories such as with regard to a semiconductor disk pack featuring plural flash

memory chips, as one example thereof. Independent claims 1 and 16 set forth a semiconductor storage apparatus to be coupled with a systems bus, an example of which is shown in Fig. 1 of the drawings, although not to be construed as being limited thereto. The plurality of nonvolatile semiconductor memories are illustrated with regard to the semiconductor disk pack 4 which shows an arrangement of flash memories or flash memory chips. The plural nonvolatile semiconductor memories (e.g. 4 in Fig. 1, etc.) are provided to store sectors of data therein (e.g., each sector of data is identified as including 512 bytes such as discussed on page 15, line 5, et. seq., of the specification). A control module, an example of which is illustrated by the processor 2 and address controller 31 in Fig. 1, is coupled with the system bus (STD BUS 1) and the non-volatile semiconductor memories 4.

Independent claims 1 and 16 are particularly directed to that aspect of operation of the nonvolatile semiconductor memories relating to an improved erase operation an example of which is described on page 16, line 12, to page 19, line 6, of the specification in conjunction with the example embodiment in Fig. 1 of the drawings and the corresponding flow chart of the improved erase operation in Fig. 4 of the drawings. Specifically, the following key aspects of the invention are included in claims 1 and 16:

> wherein said control module refers to a table for selecting a first one of said nonvolatile semiconductor memories and sends a first erase command to said first one of said nonvolatile semiconductor memories to initiate a first internal erase operation of data within said first one of said nonvolatile semiconductor memories,
>
> wherein, after said first erase command has been sent, said control module sends a second erase command to a second of said nonvolatile semiconductor memories, different from said first one of said nonvolatile semiconductor memories to which said first erase command was sent, to initiate a second internal erase operation of data within said second of said nonvolatile semiconductor memories while said first one of said nonvolatile semiconductor memories is still

performing said first internal erase operation responsive to said first erase command,

wherein said control module updates a designation of the nonvolatile semiconductor memories in the table after each occurrence of sending an erase command to a respective nonvolatile semiconductor memory, and

wherein said control module executes status polling from the nonvolatile semiconductor memory to which said first erase command has been sent and is followed by executing status polling from the second nonvolatile semiconductor memory to which said second erase command has been sent.

Regarding the set forth "control module refers to a table for selecting a first one of said nonvolatile semiconductor memories and sends the first erase command to said first one of said nonvolatile semiconductor memories to initiate a first internal erase operation of data within said first one of said nonvolatile semiconductor memories", the discussion on page 17, line 10 et. seq., and Fig. 3 of the specification, relate thereto. For Example, after having set the sectors- to-be erased in the write management table, the processor 2 sends erase commands into the respective chips of the nonvolatile memories 4 (e.g., flash memories) listed in the write management table while updating the designation of the flash memory chip in the table. Subsequently, the processor 2 determines if the next area to-be-erased exists, as is explained with regard to Steps 42-46 of the erasing procedure in Fig. 4 of the drawings and discussed on page 17, line 22, et. seq., of the Specification.

Using the example embodiment in Fig. 1 of the drawings and the erase procedure in Fig. 4, the processor 2 further executes status polling from the memory chip into which the erase command has been initially written (see step 47 in Fig. 4), so as to acknowledge if an erase process within the designated one of the nonvolatile memories 4 has ended. Subsequently, the processor determines whether or not the next management member of the table exists (see step 48 in

Fig. 4). If the next management number exists, the erase sequence returns to step 46. The above-discussed featured aspects relating to the erasing of data from the nonvolatile semiconductor memories with regard to the schemed construction disclosed in the example Fig. 1 embodiment and described with regard to Fig. 4, although not to be construed as being limited thereto, are now specifically set forth with regard to the four "wherein" clauses in independent claim 1 and, similarly, in independent claim 16.

It is submitted, the invention as now set forth in claim 1 and the dependent claims thereof as well as that according to claim 16 and the dependent claims thereof, were not taught nor could have been realizable from the combination of Nishi (USP 5,724,544) and Robinson et al (USP 5,388,248), and as alleged in the outstanding rejection (based on the alleged combined teachings of these references).

It is submitted both Nishi and Robinson et al failed to teach or suggest a semiconductor storage apparatus construction including a control module configured to send successive erase commands and which further calls for updating the designation of the nonvolatile semiconductor memory in the table after each occurrence of sending an erase command to a respective nonvolatile semiconductor memory as well as performing successive status polling, in accordance with claims 1+ and 16.

It is alleged by the Examiner that the set forth limitations contained in the first and second "wherein" clauses in claims 1 and 16 are covered by the combined teachings of Nishi and Robinson et al. Nishi, which is the primary reference applied in the rejection, discloses a schemed construction in which for a rewriting data operation, the memory controller 208 delivers an erase signal EE1 to the byte

rewriting EEPROM 30 before the write signal is sent so as to erase data existing in the address which is to be rewritten (see col. 4, lines 19-22). Such is similarly performed with regard to the memory controller 210 which sends an erase signal EE2 to the flushing EEPROM 40 to erase all the data stored in the data area (see col. 4, lines 29-30). However, there does not appear to be any teaching in Nishi of sending a first and second erase command by the control module such that:

> wherein, after said first erase command has been sent, said control module sends a second erase command to a second of said nonvolatile semiconductor memories, different from said first one of said nonvolatile semiconductor memories to which said first erase command was sent, to initiate a second internal erase operation of data within said second of said nonvolatile semiconductor memories **while said first one of said nonvolatile semiconductor memories is still performing** said first internal erase operation responsive to said first erase command.

This is specifically discussed with regard to the example embodiment Fig. 1, although not to be construed as being limited thereto, in the present specification. For example, see the discussion on page 16, line 20, et seq. Although Nishi does disclose sending separate commands to respectively different nonvolatile memories by separate memory controllers, the relationship in the timing of execution of the first erase command and that of the second erase command (according to claims 1 and 16), in which the second erase command is sent to initiate a second internal erase operation of data (within said second of said nonvolatile memories) while said first one of said nonvolatile semiconductor memories is still performing said internal erase operation...is <u>not</u> taught by Nishi.

It is also submitted that the updating of the table after each occurrence of sending an erase command to a respective nonvolatile semiconductor memory, as well as executing by the control module status polling from the nonvolatile memory (e.g., flash memory chip) to which said first erase command has been sent and

followed by executing status polling from the other nonvolatile memory to which the second erase command has been sent were not taught by Nishi nor, for that matter, in view of the combined teachings of Nishi and Robinson et al. Regarding the "signal BUSY" in Nishi, this refers to the sending by system controller 212, continuously, a busy signal to the host processor to report that processing is under way in the memory card 1 at the time of rewriting. According to Nishi, "the system controller 212 erases data by controlling the memory controllers 208 and 210 while sending a signal "BUSY" to the host processor" (see column 4, lines 32-56). It is apparent from Nishi's disclosure that the referred to "signal BUSY" is different in detail from that of the status polling of the nonvolatile semiconductor memories according to that set forth in the last "wherein" clause of independent claims 1 and 16 (see also the supportive discussion in the specification).

New claims 18-21 further characterize the set forth aspect of “status polling”. Example support thereof is found on page 7, lines 3-22, of the Specification.

Robinson, it is submitted, does not overcome the deficiencies referred to above, regarding Nishi's teachings. In this regard, the earlier discussions concerning Robinson and Nishi in the file history of the above-identified application are incorporated herein for purposes of this response. It is submitted independent claims 1 and 16 are defining over the combined teachings of Nishi and Robinson et al. Correspondingly, for the same and similar reasons as that which render claims 1 and 16 allowable, the dependent claims thereof are likewise considered to be allowable over the combined teachings of Nishi and Robinson et al.

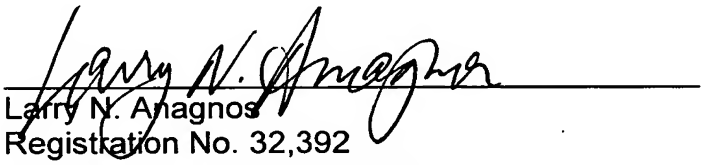
Therefore, in view of the above-made amendments together with the accompanying Remarks, withdrawal of the outstanding rejection, as well as

favorable action on pending claims 1-16, together with an early formal notification of allowance of the above-identified application, is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Docket No. 1487.32253CC8), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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